LDMOS TRANSISTOR

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of Korean Patent Application No. 10-2004-0117144, filed on Dec. 30, 2004, which is hereby incorporated by reference as if fully set forth herein.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a semiconductor device, and more particularly, to a lateral double-diffused metal-oxide-semiconductor (LDMOS) having a uniform distribution of channel impurity concentration.

[0004] 2. Discussion of the Related Art

[0005] Referring to **FIG. 1**, illustrating a conventional LDMOS transistor, an n^- semiconductor substrate **100** has active region set according to a device isolation layer **110**. A p-type body **120** and an n^- extended drain region **130** are formed in the n^- semiconductor substrate **100** to be separated from each other by a predetermined distance. An n^+ source region **140** is disposed on the p-type body **120**. A channel **121**, occurring in the p-type body **120** adjacent the n^+ source region **140**, is overlapped by a gate isolating layer **160** and a gate conducting layer **170**, which are sequentially formed atop the channel. Spacers are formed on the sidewalls of the gate conducting layer **170**. An n^+ drain region **150** is disposed on the n^- extended drain region **130**. The structure is completed by a double diffusion process in which an ion implantation process is carried out twice, i.e., once before formation of the gate spacer layer **180** and again after its formation. The source and drain regions **140** and **150** are electrically connected with a source electrode S and a drain electrode D, respectively.

[0006] **FIG. 2** shows the relative impurity concentrations with respect to the channel of the LDMOS transistor of **FIG. 1**. For example, the n^+ source region **140** exhibits an impurity concentration curve A1, which is relatively high and decreases toward the channel **121**; the channel exhibits an impurity concentration curve B1 that is relatively low and decreases toward the n^- drift region of the semiconductor substrate **100**; and the drift region exhibits a uniform impurity concentration curve C1. To obtain a desirable breakdown voltage, the channel **121** should show a uniform distribution of its ion concentration. Since a contemporary LDMOS transistor has a grade junction, however, the length of the channel **121** cannot be reduced, which limits device integration.

SUMMARY OF THE INVENTION

[0007] Accordingly, the present invention is directed to an LDMOS transistor that substantially obviates one or more problems due to limitations and disadvantages of the related art.

[0008] The present invention provides an LDMOS transistor in which an impurity concentration is uniformly distributed in a channel so as to reduce the length of the channel.

[0009] Additional advantages and features of the invention will be set forth in part in the description which follows and will become apparent to those having ordinary skill in the art upon examination of the following. These and other advantages of the invention may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0010] To achieve these and other advantages in accordance with the invention, as embodied and broadly described herein, there is provided a lateral double-diffused MOS transistor comprising a drift region of a first conductivity; a body of a second conductivity, the body being disposed in the drift region and having a channel thereon; and a source region of the first conductivity, the source region being disposed within the body and having an upper region surrounded by a first impurity region of the first conductivity.

[0011] It is to be understood that both the foregoing general description and the following detailed description of the present invention are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The accompanying drawings, which are included to provide a further understanding of the invention illustrate exemplary embodiments of the invention and together with the description serve to explain the principle of the invention. In the drawings:

[0013] **FIG. 1** is a sectional view of a conventional LDMOS transistor;

[0014] **FIG. 2** is a graph illustrating impurity concentration with respect to the channel of the LDMOS transistor of **FIG. 1**;

[0015] **FIG. 3** is a sectional view of an LDMOS transistor according to the present invention; and

[0016] **FIG. 4** is a graph illustrating impurity concentration with respect to the channel of the LDMOS transistor of **FIG. 3**.

DETAILED DESCRIPTION OF THE INVENTION

[0017] Reference will now be made in detail to exemplary embodiments of the present invention, examples of which are illustrated in the accompanying drawings. Wherever possible, like reference designations will be used throughout the drawings to refer to the same or similar parts.

[0018] Referring to **FIG. 3**, illustrating an LDMOS transistor according to the present invention, an n^- semiconductor substrate **200** has an active region defined by a device isolation layer **210**. The n^- semiconductor substrate **200** serves as a drift region, and if necessary, such a drift region may be specifically formed. A p-type body **220** and an n^- extended drain region **230** are formed in the n^- semiconductor substrate **200** to be separated from each other. The p-type body **220** and an n^- extended drain region **230** can be separated by a predetermined distance. An n^+ source region **240** is disposed within the p-type body **220** and has an upper region surrounded by an n^- first impurity region **241**. The disposition of the n^- first impurity region **241**, which has a